IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

REPLY BRIEF

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Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant hereby replies to the Examiner's Answer, mailed March 25, 2004, in an Appeal of the final rejection of claims 1 through 16 in the above-identified patent application.

REAL PARTY IN INTEREST

A statement identifying the real party in interest is contained in Appellant's Appeal Brief.

RELATED APPEALS AND INTERFERENCES

A statement identifying related appeals is contained in Appellant's Appeal Brief.

STATUS OF CLAIMS

A statement identifying the status of the claims is contained in Appellant's Appeal Brief.

STATUS OF AMENDMENTS

A statement identifying the status of the amendments is contained in Appellant's Appeal Brief.

5

SUMMARY OF INVENTION

A Summary of the Invention is contained in Appellant's Appeal Brief.

ISSUES PRESENTED FOR REVIEW

A statement identifying the issues present for review is contained in

10   Appellant's Appeal Brief.

GROUPING OF CLAIMS

The rejected claims stand and fall together.

15

CLAIMS APPEALED

A copy of the appealed claims is contained in an Appendix of Appellant's Appeal Brief.

ARGUMENT

20   In the Examiner's answer, the Examiner asserts that it is not claimed or disclosed in the present application that the allocation of instructions is done independently of the type of instruction ready for execution within each thread. The Examiner further asserts that the statement on page 6, lines 21-23, teaches that the functional units are independently allocated to the threads and does not teach that the

25   allocation is independent of the instruction type.

Appellants note that, in order to *independently* allocate functional units to threads, the allocation *must* be independent of the instruction type. If this were not the case, the allocation would depend on the instruction type and, therefore, the allocation of a functional unit to a thread would *depend* upon the type of instruction ready for

30   execution in said thread. Stated another way, a thread would determine which functional

units could be allocated to it. Thus, the allocation of the functional units would be *dependent on, and not independent of,* the threads.

The Examiner further asserts that claims 5-7 clearly set forth "that the instructions are allocated based on the availability of functional unit." Appellants agree

5   that, inherently, only functional units that are available (i.e., functional units that are unallocated) will be allocated. When the unallocated functional units are allocated, they will be independently allocated to the threads.

The Examiner further asserts that the identification of functional units and registers for the fetched instructions is conventionally done on the basis of the type of

10   instruction. The Examiner, however, is not interpreting the identification step within the context of the present invention. During the allocation process, even though the functional units do not correspond to particular instruction types, a particular functional unit must be identified so that it can be allocated to a thread. For example, if a thread A requires a functional unit, the allocation mechanism must identify the allocated functional

15   unit by a name or number in order for the instructions of thread A to be forwarded to the proper functional unit. Thus, the step of identifying functional units and registers does not infer that the functional units are allocated on the basis of an instruction type.

Conclusion

20   The rejections of the independent claims under section §102 in view of Chung et al. are therefore believed to be improper and should be withdrawn. The rejected dependent claims are believed allowable for at least the reasons identified above with respect to the independent claims.
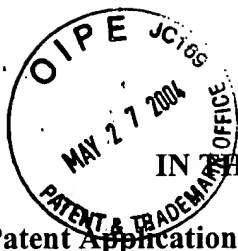
The attention of the Examiner and the Appeal Board to this matter is

25   appreciated.

Respectfully,

Kevin M. Mason

Date: May 25, 2004   Kevin M. Mason
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	Berenbaum et al.
Case:	7-2-3-3
Serial No.:	09/538,670
Filing Date:	March 30, 2000
Group:	2154
Examiner:	Larry D. Donaghue

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Signature: _____ Date: May 25, 2004

Title: Method and Apparatus for Allocating Functional Units in a Multithreaded VLIW Processor

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Sir:

Submitted herewith are the following documents relating to the above-identified patent application:

(1) Reply Brief (original and two copies).

In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0762** as required to correct the error. A duplicate copy of this letter and two copies of the Reply Brief are enclosed.

Respectfully,

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Date: May 25, 2004